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[54] **PHYSICAL ADDRESS SIZE SELECTION AND PAGE SIZE SELECTION IN AN ADDRESS TRANSLATOR**

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[*] Notice: The term of this patent shall not extend beyond the expiration date of Pat. No. 5,617,554.

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[51] **Int. Cl.**[6] **G06F 12/10**

[52] **U.S. Cl.** **711/208**; 711/212

[58] **Field of Search** 395/421.02, 416, 395/418

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[57] **ABSTRACT**

An address translator and a method for translating a linear address into a physical address for memory management in a computer is described herein. Different memory sizes, and different page sizes can be selected. The address translator can translate from a standard 32-bit linear address for compatibility with previous 32-bit architectures, and can also translate to a physical memory size with a larger physical address than linear address; i.e., greater than 32 bits (e.g. 36 bits and up), with no increase in access time. The address translator translates a linear address that includes an offset and a plurality of fields used to select entries in a plurality of tables. The format of the linear address into fields is dependent upon the selected memory size and the selected page size. For a large memory size, the tables include a directory pointer table that includes a group of directory pointers, a plurality of page table directories each of which includes a group of page directory entries, and a plurality of page tables each of which includes a group of page table entries. The size of the entries in the tables is dependent upon the selected memory size. The contents of the tables are stored in memory, and furthermore the pointer table is stored in both main memory and in dedicated pointer table registers.

18 Claims, 12 Drawing Sheets